REMARKS

The Specification

The first paragraph of the specification has been amended to incorporate the Serial Number of the related U.S. Provisional Patent Application. The paragraphs under the Summary of the Invention and Advantages section have been amended to coincide with the Amendments to the independent claims, which are set forth in greater detail below. Various paragraphs under the Detailed Description of the Preferred Embodiment section have been amended to coincide with terminology changes and other amendments to the claims, which are also set forth in greater detail below. The Specification has also been amended to ensure consistent use of terminology. It is respectfully submitted that no new matter is being introduced.

The Claims

Claims 1-10, 12, and 14-47 remain in the Application with Claims 1 and 19 being in independent form. Claims 11, 13 and 48-67 have been cancelled. Claims 1-10, 12, 14, 16-19, 25, 27-28, 30-34, 38-40, 43, 45 and 47 are currently being amended with claims 15, 20-24, 26, 29, 35-37, 41-42, 44, and 46 remaining unchanged. The claim amendments have been made to further clarify the scope of the invention, address the rejections made by the Examiner, and to distinguish the subject invention from the cited prior art.

Applicant thanks the Examiner for the thorough review of the Specification and Claims of the subject Application. Each of the Examiner's rejections and objections are

addressed separately below.

Claim Objections

Claim 18 is objected to due to a typographical error. Claim 18 has been amended to correct this typographical error such that this Objection is believed overcome.

Claim Rejections – 35 U.S.C. § 112

The Examiner contends that Claim 9 is not enabled by the specification as filed. In particular, the Examiner contends that the specification fails to disclose how creating a virtual memory map of each of the codes may be done, "such that the first and second processors can address and forward processed information to each of the index processors within the system." The discussion of the virtual memory map and the utilization of these maps is discussed throughout the specification. The Examiner correctly identifies page 10, line 24 to page 11, line 1 as a portion of the specification that discusses the virtual memory map and its operation. Applicant also directs the Examiner to Figures 4, 6, 16, and 19, which illustrate the virtual memory maps having the codes[1] of each of the processors of the nodes. Further, other sections of the specification that discuss the operation of the virtual memory map in greater detail are at page 15, line 19 to page 16, line 3; page 17, lines 18-20; page 19, lines 17-23; page 20, lines 1-10; and page 22, lines 2-17.

The virtual memory map is a means by which the nodes can recognize and address

[1]As is subsequently discussed, the term "Code" has been changed to - -identifier- -.

each of the other nodes in the system. Hence, the processed information is transmitted by utilizing the virtual memory map of the sending nodes. The processor in a particular node does not recognize the difference between its own real memory and the virtual memory map. Hence, the node does not know the difference between writing to its own real memory or writing to the real memory location of another node through the virtual memory map. As best shown in Figure 16, a data destination pointer directs the flow of the processed information to the virtual memory map and points to a destination node. The destination address corresponding to the destination node of the virtual memory map is then assigned to the processed information. In the example of Figure 16, the data destination pointer directs the processed information to node 2 in the virtual memory map such that the destination address of node 2 will be assigned to this information. Having identified the portions of the application that fully describe the operation of the virtual memory map, the rejection of Claim 9 is believed overcome.

Claim 18 is also rejected for failing to comply with the enablement requirement. In particular, the Examiner contends that the specification fails to provide support for "limiting the number of times that the processed information can be sent from a sending processor." The Examiner also contends that the specific claim language does not appear in the specification and no mechanism is described which would limit the number of times that the processed information can be sent from a processor of a sending node. Applicant directs the Examiner to page 15, lines 1-5, which discuss a counter for controlling the number of times that processed information can be sent to an addressed node. This portion of the specification has been amended to specifically recite the language as set forth in Claim 18 as

originally filed. This rejection to Claim 18 is therefore believed overcome.

The Examiner is unsure if Claims 8 and 27 are to further define a previous claim or to be an additional step to a previous claim. Each of these claims simply redefine a feature of their corresponding independent claims. In particular, the independent claims indicate that an indexer indexes the nodes to define different destination addresses. Claims 8 and 27 further define the operation of the indexer by setting forth that the indexer indexes the nodes to define a code (identifier) for each of the nodes. In other words, the destination addresses are now further defined as codes.

The Examiner also contends that Claims 8 and 27 are unclear due to the term "code". Applicant has changed this term to eliminate any potential confusion. In particular, the term "code" has been changed to "identifier". As discussed in the first paragraph under the Detailed Description section, examples of a code (now identifier), are numerical indicators 1 through 6. As also mentioned, any suitable numeric indicator may be used to differentiate one node from another. Hence, the identifiers are simply a way to differentiate the nodes from each other. In accordance with the discussion above and the amendments to the claims, the rejections to Claims 8 and 27 are believed overcome.

Claims 10, 12, 30 and 32 are rejected as being indefinite due to the use of the term "indicative of". The claims and specification have been amended to change this terminology to "corresponding to" to avoid any potential confusion. Hence, an address of the processed information corresponds to the identifier of the addressed node. Taking the customary use of the term "corresponding", it is clear that the claimed language identifies that the destination address is an equivalent or in conformity with the identifier. The

rejections of these claims based on indefiniteness is therefore believed overcome.

The Examiner also rejected Claims 12 and 32 based on some apparent confusion with the term "memory address". The claims and specification have been amended to clarify the term "memory address" and the operation of assigning of the memory address. The assigning of the memory address, as set forth in Claim 12, is a further or additional step in addition to the step of assigning a destination address. The memory address corresponds to a location of the real memory in the addressed node. Discussion of the memory address as it relates to the locations of the real memory are located at page 10, lines 14-16 and page 21, lines 1-3. In light of the amendments to Claims 12 and 32 and the remarks set forth above, the rejections to these claims is believed overcome.

The Examiner contends that it is unclear in Claim 39 how the destination pointer is capable of sending processed information. Applicant has amended this claim and the specification to clarify that the destination pointer directs a sending processor to send processed information. Support for this amendment is found in page 11, lines 16-19; page 18, lines 20-21; page 19, lines 17-19; page 20, lines 8-10; and page 22, lines 2-9. Having amended Claim 19 and explained the support for this claim, the rejection of Claim 39 is believed overcome.

The Examiner objects to Claims 39 and 40 as being unclear due to a issue with the term "pair". These claims have been amended to avoid any clarity issues and as such these objections are believed overcome.

Finally, the Examiner rejects Claim 43 as being unclear. Applicant has amended this claim to clarify the operation of the counter such that it is possible for processed

information to be sent a number of times to an addressed node.

Claim Rejections – 35 U.S.C. § 102

Claims 1-3, 5-6, 8, 19-21, 27, 36-37, and 47 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Antonov (U.S. Patent No. 5,884,046). Claims 14-17, 33,-35, 41-42, and 45-46 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Antonov. Claims 4, 9-13, 18, 22-26, 28-32, 38-40, and 43-44 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Antonov in view of various additional prior art references. Claim 7 was not formally rejected such that this claim is believed to be in condition for allowance.

Independent Claims 1 and 19 have been amended to clarify these claims and to clearly distinguish these claims over the prior art of record. In particular, these claims have been amended to set forth a first node having the first processor and a first real memory location as well as a second node having the second processor and a second real memory location. Support for these claims amendments is found throughout the specification and the drawings as filed. Amendments to many of the dependent claims was necessitated by the incorporation of the first and second nodes into the independent claims.

Claims 1 and 19 have also been amended to set forth that the processed information sent from the first processor toward the hub is accomplished *without storing the processed information in the first real memory location of the first node*. Similarly, as set forth in Claim 19, the processed information sent from the second processor toward the hub is accomplished *without storing the processed information within the second real memory location of the second node*. Further, the processed information is stored within the real

memory location associated with the addressed node. Support for these claim amendments is found at page 14, lines 15-16 and at page 21, lines 6-13. These claim amendments clearly distinguish the independent claims from Antonov as well as the remaining prior art of record. Many of the dependent claims have also been amended to clarify these claims and to conform the language of these claims to the language of Claims 1 and 19.

Regarding Antonov, this patent discloses a network server and switch which is more analogous to a conventional network computing environment. Hence, Antonov is at another level and is an application of a multi-processing system. The connections between the work stations, or nodes, and the network switch/server are conventional local area network links. Networks typically employ a multi-layer communication structure implemented in software and hardware to pass information to and from a node to the network. By their very nature, these communication links include significant overhead or burden and dramatically impact the latency of a message between sender and recipient. As discussed at column 6, line 64 through column 7, Antonov specifically mentions that it is necessary to maintain identical copies of the data in different processing nodes. Column 10, lines 15-44 describes storing and sending copies of data to the requesting node. At all times, retrieving data means taking a copy of the data. This additional storing of data and monitoring of data (to verify accuracy), greatly increases the overhead of the system and dramatically impacts the latency or speed of the message between the sender and the recipient.

The other references of record operate in a similar manner. For example, the Blumrich article is a good illustration of a reflective memory system. As discussed at page 5, column 2, Blumrich discusses maintaining consistent copies of data. Also, page 11,

column 1, mentions "automatic replication of data structures to remote processes". Hence, reflective memory systems also store the data before it is sent, i.e., a copy is being sent. Again, this duplication of data greatly reduces the effectiveness and speed of the system. Enclosed herewith is another article, entitled "Towards A More Efficient Reflective Memory For The PC-Based DSM", that further discusses reflective memory and specifically mentions Blumrich.

The subject invention, however, is a send and forget type system. As set forth in independent Claims 1 and 19, the processed information (data) is not saved at the sending node. The processed information is only directed to the virtual memory map and no local copy is retained. There are no retry and resend mechanisms in the subject invention. Hence, there is no possibility for signal contention or deadlock, which can occur with network systems. The technique of the subject invention guarantees very low latency without the possibility of data collisions or the intervention of network protocols.

In accordance with the claim amendments and the remarks set forth above, independent Claims 1 and 19 are believed to be in condition for allowance. Claims 2-10, 12, 14-18, and 20-47 are also believed to be allowed as these claims depend from the unique features of independent Claims 1 or 19.

The remaining references cited but not applied to the claims have been considered. Since the Examiner has apparently considered these references as less pertinent than the above discussed references, further discussion of the non-applied references, at this time, is considered unnecessary. However, it is respectfully submitted that the claims in the subject patent application patentably define over all references of record either independently or in

combination.

Accordingly, it is respectfully submitted that the Application, as amended, is now presented in condition for allowance, which allowance is respectfully solicited. The Commissioner is authorized to charge our Deposit Account No. 08-2789 for any fees or credit the account for any overpayment.

Respectfully submitted,

HOWARD & HOWARD ATTORNEYS, P.C.

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Date

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CERTIFICATE OF EXPRESS MAILING

I hereby certify that the enclosed **AMENDMENT, PETITION FOR A THREE MONTH EXTENSION OF TIME,** and a **SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT with attached PTOSB08A and noted publications** are being deposited with the United States Postal Service as Express Mail, postage prepaid, in an envelope as "Express Mail Post Office to Addressee", Mailing Label No. **EV612878066US** and addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450 on **June 16, 2005.**

Anne L. Kubit